KIA
SEMICONDUCTORS

-7.5A, -30V
P-CHANNEL MOSFET

7P03A

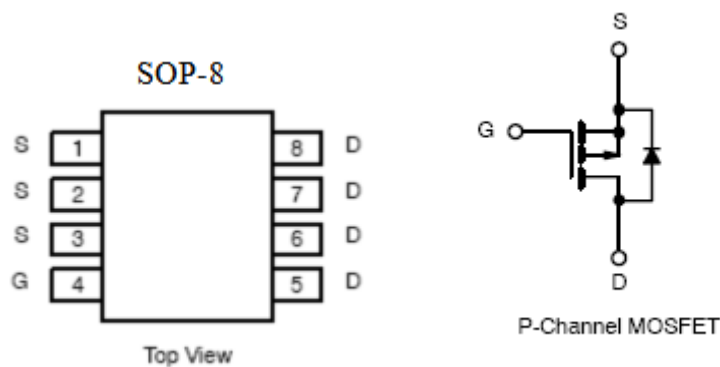## 1. Features

- n $R_{DS(on)}$=18mΩ(typ)@ V_{GS}=-10 V

- n   Super low gate charge

- n   Green device available

- n   Excellent Cdv/dt effect decline

- n   Advanced high cell density trench technology

2. Description

The KIA7P03A is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KIA7P03A meet the RoHs and Green Product requirement.

3. Symbol

SOP-8

Top View

P-Channel MOSFET

4. Absolute maximum ratings

(T_A=25°C,unless otherwise noted)

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	-30	V
Gate-source voltage		V_{GS}	±20	V
Continuous drain current V_{GS} @-10V[1]	T_A=25°C	I_D	-7.5	A
	T_A=70°C		-6	
Pulsed drain current[2]		I_{DM}	-50	A
Single pulse avalanche energy[3]		EAS	72.2	mJ
Avalanche current		I_{AS}	-38	A
Total power dissipation[4]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2	W
Junction and storage temperature range		T_J,T_{STG}	-55 to150	°C
Thermal resistance-junction to ambient[1]		$R_{θJA}$	75	°C/W
Thermal resistance-junction to ambient[1] (t≤10s)			40	
Thermal resistance-junction to case[1]		$R_{θJC}$	24	

5.Electrical characteristics

(T$_J$=25°C,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source breakdown voltage	BV$_{DSS}$	V$_{GS}$=0V, I$_D$=-250µA	-30	-	-	V
BV$_{DSS}$ Temperature coefficient	$\triangle$BV$_{DSS}$/ $\triangle$T$_J$	Reference to 25 °C, I$_D$=1mA	-	0.022	-	V/ °C
Drain-Source Leakage Current	I$_{DSS}$	V$_{DS}$=-24V,V$_{GS}$=0V, T$_J$=25°C	-	-	-1	µA
		V$_{DS}$=-24V,V$_{GS}$=0V, T$_J$=55°C	-	-	-5	
Gate-source leakage current	I$_{GSS}$	V$_{GS}$=$\pm$20V,V$_{DS}$=0V	-	-	$\pm$100	nA
Gate threshold voltage	V$_{GS(th)}$	V$_{DS}$=V$_{GS}$, I$_D$=250µA	-1	-	-2.5	V
V$_{GS(th)}$Temperature coefficient	$\triangle$V$_{GS(th)}$		-	4.6		mV/°C
Static drain-source on- resistance[2]	R$_{DS(on)}$	V$_{GS}$=-10V,I$_D$=-6A	-	18	20	mΩ
		V$_{GS}$=-4.5V,I$_D$=-4A	-	27	32	
Forward transcend ductance	g$_{FS}$	V$_{DS}$=-5V, I$_D$=-6A	-	17	-	S
Gate resistance	R$_g$	V$_{DS}$=0V, V$_{GS}$=0V, f=1.0MHz	-	13	-	Ω
Total gate charge(-4.5V)	Q$_g$	V$_{DS}$=-15V, V$_{GS}$=-4.5V I$_D$ =-6A	-	12.6	-	nC
Gate-source charge	Q$_{gs}$		-	4.8	-	
Gate-drain charge	Q$_{gd}$		-	4.8	-	
Turn-on delay time	t$_{d(on)}$	V$_{DD}$=-15V, R$_G$=3.3Ω, V$_{GS}$=-10V I$_D$=-6A	-	4.6	-	ns
Rise time	t$_r$		-	14.8	-	
Turn-off delay time	t$_{d(off)}$		-	41	-	
Fall time	t$_f$		-	19.6	-	
Input capacitance	C$_{iss}$	V$_{GS}$=0V, V$_{DS}$=-15V F=1.0MHZ	-	1345	-	pF
Output capacitance	C$_{oss}$		-	194	-	
Reverse transfer capacitance	C$_{rss}$		-	158	-	
Diode characteristics						
Continuous source current[1.5]	I$_S$	V$_G$=V$_D$=0V,Force current	-	-	-7.5	A
Pulsed source current[2.5]	I$_{SM}$		-	-	-50	A
Diode forward voltage[2]	V$_{SD}$	V$_{GS}$=0V,I$_S$=-1A, T$_J$=25°C	-	-	-1.2	V
Reverse recovery time	t$_{rr}$	I$_F$=-6A,dI/dt=100A/us, T$_J$=25°C	-	16.3	-	nS
Reverse recovery charge	Q$_{rr}$		-	5.9	-	nC

Note:1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse width ≤300us,duty cycle ≤2%.

3. The EAS data shows Max.rating. The test condition is V$_{DD}$=-25V, V$_{GS}$=-10V, L=0.1mH, I$_{AS}$=-38A.

4. The power dissipation is limited by 150 °C junction temperature.

5. The data is theoretically the same as I$_D$ and I$_{DM}$, in real applications, should be limited by total power dissipation.
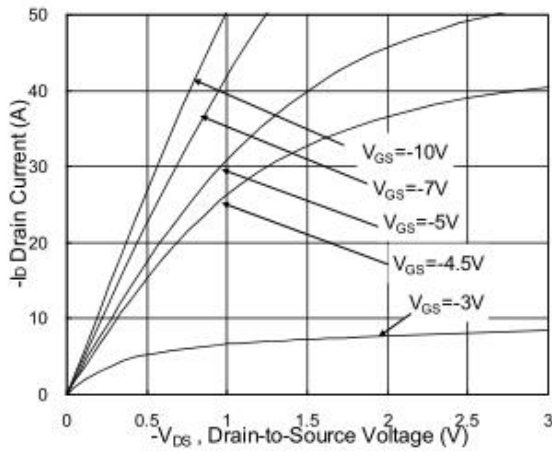
6. Test circuits and waveforms
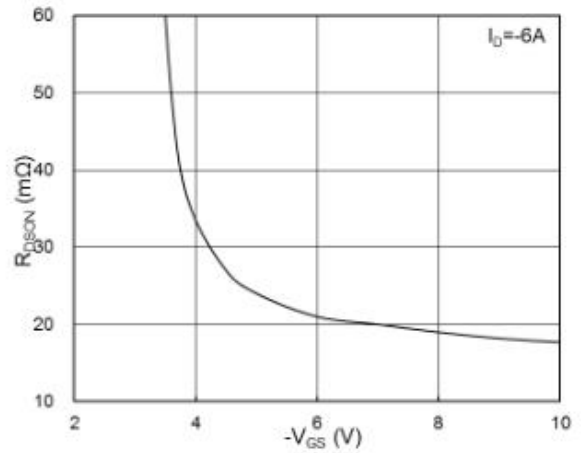

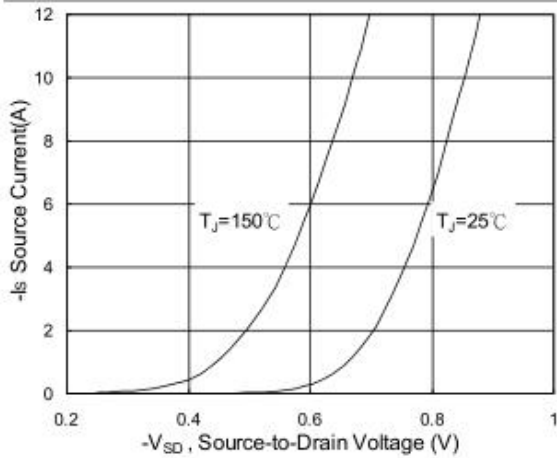**Fig.1 Typical Output Characteristics**

Fig.2 On-Resistance v.s Gate-Source

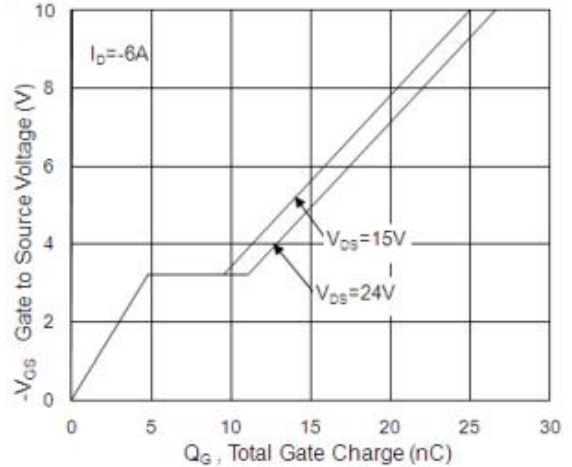**Fig.3 Forward Characteristics of Reverse**

Fig.4 Gate-Charge Characteristics

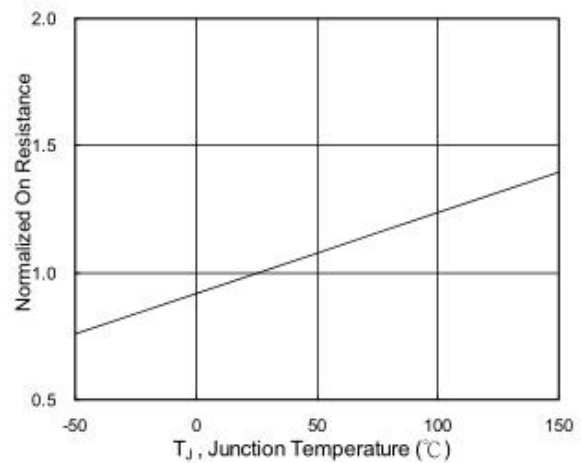**Fig.5 Normalized V$_{GS(th)}$ vs. T$_J$**

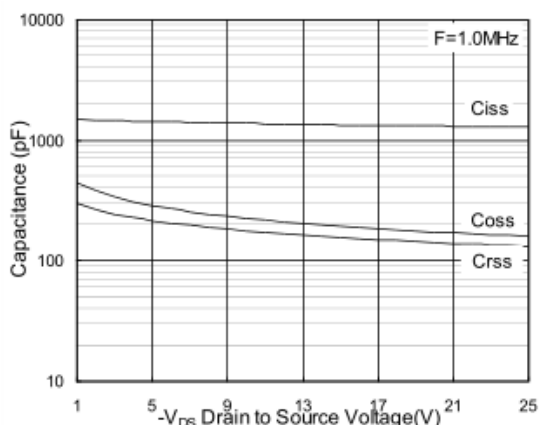**Fig.6 Normalized R$_{DSON}$ vs. T$_J$**
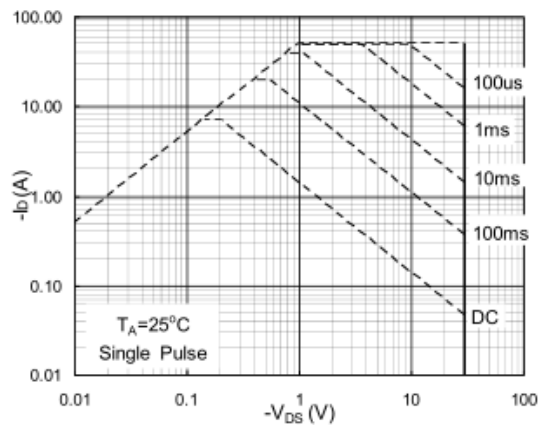
Fig.7 Capacitance
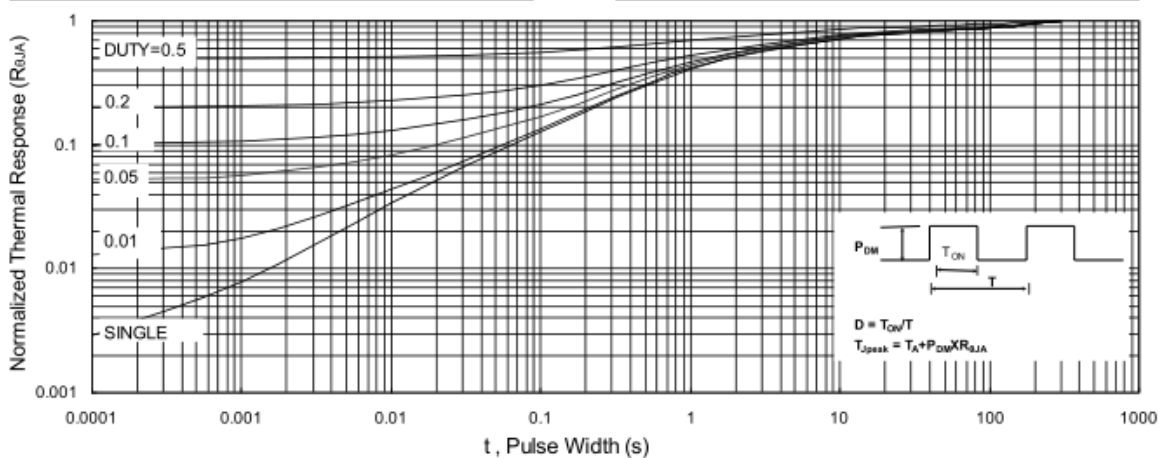

Fig.8 Safe Operating Area

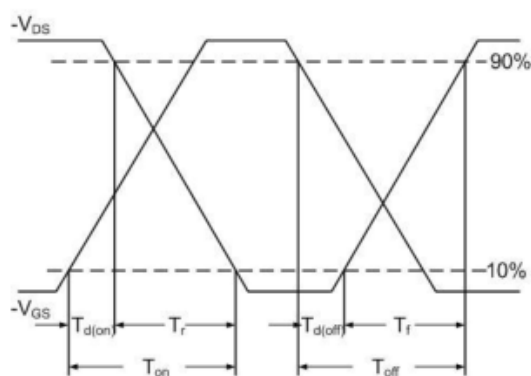**Fig.9 Normalized Maximum Transient Thermal Impedance**
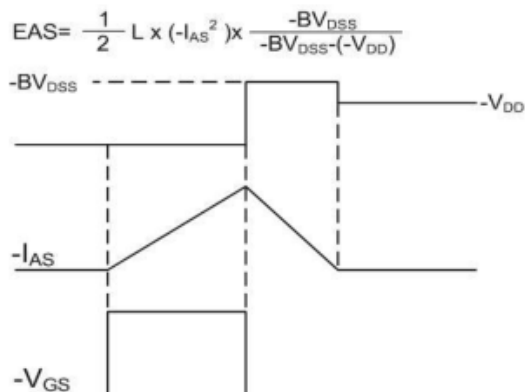

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Switching Waveform

$$EAS= \frac{1}{2} L \times (-I_{AS}^2) \times \frac{-BV_{DSS}}{-BV_{DSS}-(-V_{DD})}$$